A CAD Methodology for Optimizing Transistor Current and Sizing in Analog CMOS Design

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EEC214
Current
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Transistor-level design methodology

- Design methodology
  - Select a circuit topology
  - Select desired performance specifications
  - Computerized optimization to select MOS currents and sizings to meet specs
  - Can also simulate topology over a range of currents and sizings and explore tradeoffs

- Transistor-level design methodology
  - Allows designer to pre-select near-optimal drain currents and sizings for any circuit
  - Considers transconductance $g_m$ and output conductance $g_{ds}$
  - Permits design in weak, moderate, or strong inversion
MOS Inversion Coefficient

- Traditionally, degrees of design freedom are drain current $I_D$, channel width $W$ and channel length $L$.
- Here, degrees of freedom are drain current $I_D$, channel length $L$ and inversion level $IC$, which is a normalized measure of $I_D$ describing level of channel inversion.

\[
IC = \frac{I_D}{2n\mu C_{ox}(W/L)U_T^2}
\]

\[
n = \frac{(COX + VDEP)}{COX},
\]

\[
U_T = \frac{kT}{q}
\]

- Weak inversion: $IC < 0.1$ ($V_{GS} - V_T \approx -72\text{mV}$)
- Moderate inversion center: $IC = 1.0$ ($V_{GS} - V_T \approx 40\text{mV}$)
- Strong inversion: $IC > 10$ ($V_{GS} - V_T \approx 220\text{mV}$)
Performance Tradeoffs – MOS Operating Plane

\[ IC_0 = \frac{I_D}{2n_0\mu_0 C_{ox} (W/L)U_T^2} = \frac{I_D}{I_0 (W/L)} \]

- Fix n0 at moderate inversion, mu0 at low field value.
- I0 is technology current

- Best C and intrinsic-gain bandwidth \( f_T \) at high IC, small L.
- Opposite for intrinsic gain, dc match, flicker noise.
- \( V_{DSAT}, g_m, \) white noise optimal at low IC.
- \( g_m \) linearity best at high IC
MOS Sizing Relationships

• If IC is increased ($I_D$ and $L$ fixed), ($W/L$) ratio, $W$, gate area (and $C_{OX}$), decrease inversely with increasing IC.

• If $L$ is increased ($I_D$ and IC fixed), $W$ increases directly with $L$ to maintain ($W/L$) ratio. Since $W$ increases, gate area (and $C_{OX}$) increases as square of increasing $L$.

• If $I_D$ increased (IC and $L$ fixed), ($W/L$) ratio, $W$, and gate area (and $C_{OX}$) increase directly with increasing $I_D$. 

MOS DC Bias Voltage and Small-Signal Parameter Relationships

- Weak/moderate inversion best for maximizing $g_m$ and minimizing white noise
- Long channel length $L$ results in higher $V_A$ and subsequently lower output conductance $g_{ds}$ → higher $r_{ds}$
Gain and Bandwidth

- Intrinsic gain is highest at weak inversion with long channel length \( L \).
- Intrinsic gain is lowest at strong inversion with short channel length \( L \).

\[
A_{v1} = \frac{g_m}{g_{ds}} = \frac{I_D (g_m / I_D)}{I_D (g_{ds} / I_D)} = \frac{I_D / V_{gm}}{I_D / V_A} \approx \frac{V_A}{V_{gm}}
\]

\[
\approx \frac{VAL \cdot L}{nU_T (\sqrt{0.25 + IC + 0.5})}
\]

**TABLE III**
MOS Gain and Bandwidth Relationships

<table>
<thead>
<tr>
<th>Parameter</th>
<th>( IC_0 \uparrow )</th>
<th>( L \uparrow )</th>
<th>( I_C \uparrow )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W_0 \text{ and } L ) are effective dimensions.</td>
<td>( L, I_D \text{ fixed} )</td>
<td>( L \uparrow )</td>
<td>( I_C, I_D \text{ fixed} )</td>
</tr>
<tr>
<td>Intrinsic Gain(^{1,2}):</td>
<td>Unchanged, W.I.(^2)</td>
<td>( \uparrow \propto L^{1,2} )</td>
<td>( \downarrow \propto \frac{1}{\sqrt{IC}} ), S.I.(^{1,2})</td>
</tr>
</tbody>
</table>
Gain and Bandwidth cont’d

- Best BW at high IC0, short L
- Velocity saturation at high IC0, short L, causing BW to limit

Intrinsic Bandwidth:\(^1\):

\[
f_n = \frac{g_m}{2\pi(C_{gs} + C_{gbi})}
\]

\[
= \frac{IC_0}{\sqrt{0.25 + IC + 0.5}} \cdot \frac{I_0}{nU_T
\]

\[
\frac{2\pi(C_{gs} + C_{gbi})L^2C_{OX}}{2\pi(C_{gs} + C_{gbi})L^2C_{OX}}
\]

\[
C_{gs} = \frac{C_{gsi}}{WLC_{OX}} = \frac{0}{3}, \frac{1}{3}, \frac{2}{3}, \text{ for W.I., M.I., S.I.}
\]

\[
C_{gbi} = \frac{C_{gbi}}{WLC_{OX}} = \frac{[\frac{3}{3}, \frac{2}{3}, \frac{1}{3}]}{n-1}, \text{ for W.I., M.I., S.I}
\]
DC Mismatch and Gate-Referred Flicker Noise

- Since mismatch dependant on $I_D$. Normalization of ID offset required for different ID
- $I_D$ current mismatch optimized at long L, low IC.
- In strong inversion, ID mismatch almost independent of IC

Threshold Voltage Mismatch:

\[
\Delta VTO = \frac{AVTO}{\sqrt{WL}} = \frac{\sqrt{IC_0}}{L} \sqrt{I_D} AVTO
\]

Transconductance Efficiency\(^2\):

\[
\frac{g_m}{I_D} \approx \frac{1-e^{-\sqrt{IC}}}{nU_T \sqrt{IC}} \approx \frac{1}{nU_T\left(\sqrt{IC} + 0.25 + 0.5\right)}
\]

\(\uparrow \propto \sqrt{IC_0}\)

\(W/L \propto \frac{1}{IC_0}\)

Unchanged, W.I.

\(\downarrow \propto \frac{1}{\sqrt{IC}}\)

S.I.\(^2\)
DC Mismatch and Flicker Noise

- $I_D$ mismatch due to threshold voltage mismatch
- DC mismatch and input-referred flicker noise voltage are minimized by maximizing gate area.
- Operating in weak IC and long L is also where max MOS gain is obtained

| Parameter | $IC \uparrow$ | $L \uparrow$ | $I_D \uparrow$
|-----------|--------------|-------------|-------------|
| Threshold Voltage Mismatch: | $\Delta V_{TO} = \frac{AV_{TO}}{\sqrt{WL}} = \frac{\sqrt{IC_0}}{L} \sqrt{\frac{I_0}{I_D} \cdot AV_{TO}}$ | $\uparrow \propto \sqrt{IC_0}$ | $\downarrow \propto \frac{1}{L}$ | $\downarrow \propto \frac{1}{\sqrt{I_D}}$
| (generally negligible for $IC < 100$) | (WL $\propto \frac{1}{IC_0}$) | (WL $\propto L^2$) | (WL $\propto I_D$) |
| Transconductance Factor Mismatch: | $\Delta K_P = \frac{AK_P}{\sqrt{WL}} = \frac{\sqrt{IC_0}}{L} \sqrt{\frac{I_0}{I_D} \cdot AK_P}$ | | | |
| Body-Effect Factor Mismatch: | $\Delta \gamma = \frac{AGAMMA}{\sqrt{WL}} = \frac{\sqrt{IC_0}}{L} \sqrt{\frac{I_0}{I_D} \cdot AGAMMA}$ | | | |
| Gate-Referred Flicker Noise Voltage: | | | | |
| $S_{V_{flicker}}(f) = \frac{K_F}{C_{ox}WL \cdot f_A}$ | | | |
| $= \frac{1}{\sqrt{WL}} \frac{K_F}{\sqrt{C_{ox} \cdot f_A}}$ | | | |
| $= \frac{\sqrt{IC_0}}{L} \sqrt{\frac{I_0}{I_D} \cdot \frac{K_F}{C_{ox} \cdot f_A}}$ | | | |
CAD Design Tool

- MOS circuit performance evaluated by
  a) Linkage to commercial SPICE-like simulator that can run EKV and BSIM3 models
  b) Linkage to custom MOS model equations which may modify existing MOS model
  c) Linkage to arrays of measured MOS data
- User interface allows designer to select design parameters as well as desired performance specs and dynamically display tradeoffs using colored bar graphs.
CAD Tool Example

Illustration of NMOS Sizing Optimization

- NMOS xtr at ID = 100uA, 0.5um CMOS process
- Intrinsic voltage gain Avi > 40 V/V
  Intrinsic bandwidth fTi > 800MHz
  DC current mismatch < 1% (1 sigma) (current mirror)
  DC voltage mismatch < 1.5 mV(1 sigma) (diff. pair)
- Short L, BW met, Avi, mismatch not met.
- Long L, Avi, mismatch met, BW not met.

<table>
<thead>
<tr>
<th>Design Inputs</th>
<th>Resulting Circuit Performance</th>
</tr>
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<tbody>
<tr>
<td>ID</td>
<td>IC₀</td>
</tr>
<tr>
<td>µA</td>
<td>µm</td>
</tr>
<tr>
<td>100</td>
<td>10</td>
</tr>
<tr>
<td>100</td>
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<tr>
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<td>10</td>
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<tr>
<td>100</td>
<td>100</td>
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Conclusions

• Transistor level design methodology can produce optimal drain current and sizing for use in any analog circuit topology using ID, IC and L to find W
• Exploring the performance of a transistor operating at different inversion levels can benefit circuit performance and expand design options
• Every MOS xtr operates in the MOS operating plane from which tradeoffs between a variety of performance criteria can be explored
• CAD tools can be designed to implement advanced behavior of MOS transistors and optimize them based on the relationships established with inversion level as a design parameter
• Device optimizations can be done before circuit simulations to reduce trial and error simulations while considering high order effects

Reference: