A Simplified, Empirical Large Signal Model for SiC MESFETs

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Outline

- Background
- Objectives
- Model Description
 - Drain current
 - Parasitics
- Experimental Verification
 - S-parameters measurements
 - Harmonic power measurements
- Conclusions

Background

- Growing interest in wide bandgap semiconductor technologies (SiC and GaN)
- SiC technology features
 - High breakdown voltage \rightarrow high RF power output
 - High power density \rightarrow Self-heating effects
- Applications: PAs, mixers, oscillators ...
- Large-signal CAD model is important
- This Work
 - Cree CRF-24010 10W
 SiC MESFET



Objectives

- Develop an accurate empirical large-signal model capable of predicting
 - IV characteristics
 - Small signal S-parameters
 - Harmonic power for the first three harmonics
- Challenges
 - Obtaining accurate characterization of the device
 - Handling IV current dispersion "drooping" effects
 - Extracting intrinsic and extrinsic parasitics
 - Modeling output and input reflected harmonics
 - Minimizing model complexity

Elements of Pulsed and Static IV



Drain Current Model

- How do we handle high power current dispersion?
- Use pulsed IV characteristics (PIV)
 - Resemble static IV curves of low power devices
 - Use known models with success
 - Only good for one bias \rightarrow not for general purpose model
 - Static characteristics may be important (class A bias)
- Modify existing drain current models
 - Add dedicated parameters to account for dispersive behavior
 - Increased complexity. Parameters may not be fully exploited.
- In this work
 - Reformulate drain current equation using known mathematical modeling techniques
 - Develop mathematical model with variable order → model IV characteristics of variable complexity



- Assumes influence of Vgs and Vds on Ids are separable
- Assumes gmpk occurs at the same Vgs independent of Vds

Drain Current Equation

• Drain current equation for this model

$$Ids = Ipk(1 + tanh(\psi))$$

$$\psi = P_1(Vgs - Vpk) + P_2(Vgs - Vpk)^2 + P_3(Vgs - Vpk)^3 \dots$$

$$P1 = Q_{01} + Q_{11}(Vds) + Q_{21}(Vds)^2 + Q_{31}(Vds)^3 \dots$$

$$P2 = Q_{02} + Q_{12}(Vds) + Q_{22}(Vds)^2 + Q_{32}(Vds)^3 \dots$$

$$P3 = Q_{03} + Q_{13}(Vds) + Q_{23}(Vds)^2 + Q_{33}(Vds)^3 \dots$$

$$\vdots$$

- Use Chalmer's method to describe Vgs nonlinearity
- Coefficients Pn are each a power series of Vds
- Since gmpk, lpk, Vpk not constant across Vds, use power series to track Pn across Vds
- Effects of Vgs and Vds are not treated as separable

Drain Current Equation Advantages

- Polynomials
 - Easy to implement, coefficients easy to determine
 - Differentiable
 - Mathematical order can be configured
 - Linear channel length effects (low order)
 - Nonlinear channel length effects (high order)
- Chalmer's method for Vgs relationship → P2 is eliminated

• Possible elimination of $tanh(\alpha Vds)$ term

- linear region no different from saturation region if gmpk, Vpk and lpk modeled correctly
- gmpk, Vpk and Ipk difficult to model at low Vds
- Purely electrical characterization of Ids

 No physical or temperature varying parameters

Drain Current Model – Static IV



- Vgs=-10.0V to -4.0V, 0.5V steps, Vds=0V to 60V, 2V steps
- Accurate modeling of complex static characteristics

Drain Current Model – Pulsed IV

- Pulsed IV data using Auriga DIVA (Nanometrics)
- (Nanomeuuco,
 Same math form, variable order ≤ 0.8 allows modeling ≤ 0.7 of PIV
 - tanh(αVds) improves linear regime fit
 - PIV drain current model used in large-signal model



VGS=-10V to 1V, 1V steps, VDS=0V to 60V, 2V steps

Complete Model with Parasitics



- Uses standard large-signal model topology \rightarrow Simple
- Parasitics extracted from S-parameter measurements
- Ids parameters optimized with parasitic resistances
- Nonlinear caps modeled with Chalmer's charge eqs

S-parameter Verification

- Cree CRF-24010 biased at VDS=48.0V IDS=500mA
- Frequency range 0.1GHz to 4.0GHz at -5dBm source
- Good agreement with measured data
- Supplemental RF current generator not needed



Harmonic Power Verification



- Large signal measurement system
 - DUT driven at 2GHz from 10dBm to 36dBm
 - Output and input reflected power for three harmonics
- No impedance matching on DUT
 - Harmonic generation and power reflection
 - Generalized characterization using 50 Ohms terms

Output harmonic power



- Good agreement for three harmonics from 10dBm to 36dBm source power at 2.0GHz for DUT biased at VDS=48.0V, IDS=500mA
- Up to fundamental output power of 40dBm

Input reflected harmonic power



- Good agreement for three harmonics from 10dBm to 36dBm source power at 2.0GHz for DUT biased at VDS=48.0V, IDS=500mA
- Up to fundamental reflected power of 34dBm

Further Work - Harmonic Power



VGS

-8.5

-10

5

Conclusions

- A new, simple empirical large-signal model for SiC MESFETs presented
- Mathematically versatile drain equation combining power series with Chalmer's model
 - Static IV
 - Pulsed IV
- Large-signal SiC MESFET model can predict
 - Pulsed IV characteristics
 - S-parameters without RF current generator
 - Large signal output and input reflected power for three harmonics

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Development of our IV model

- Step 1: Take data
- Step 2: (Optional) Interpolate and extrapolate data if necessary
- Step 3: Take the derivative of Ids wrt Vgs at every Vds value. From this, find gmpk, Ipk, Vpk at every Vds.
- Step 4: Fit gmpk, lpk, Vpk wrt Vds to a polynomial
- Step 5: Guess a set of P parameters at each Vds
- Step 6: Optimize the P for every Vds. In other words, fit Ids vs Vgs curve for each value of Vds.
- Step 7: Fit the optimized P parameters as polynomial functions wrt to Vds.
- Step 8: Using the fitted parameters, compute the Ids based on the polynomial fitted Angelov model